CLAIMS

What is claimed is:

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1   1.   An apparatus comprising:

2   a storage circuit coupled to a prefetcher to store a plurality of prefetch

3   addresses, the plurality of prefetch addresses corresponding to most recent

4   access requests from a processor, the prefetcher generating an access request to

5   a memory when requested by the processor; and

6   a canceler coupled to the storage circuit and the prefetcher to cancel the

7   access request when the access request corresponds to at least P of the stored

8   prefetch addresses, P being a non-zero integer.

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1   2.   The apparatus of claim 1 wherein the storage circuit comprises:

2   a storage element to store the plurality of prefetch addresses from the

3   most recent access requests by the processor, the storage element being one of

4   a queue with a predetermined size and a content addressable memory (CAM).

1   3.   The apparatus of claim 2 wherein the queue comprises:

2   a plurality of registers cascaded to shift the prefetch addresses each time

3   the processor generates an access request.

1   4.   The apparatus of claim 3 wherein the canceler comprises:

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2   a matching circuit to match a current prefetch address associated with

3   the access request with the stored prefetch addresses.

1   5.   The apparatus of claim 4 wherein the canceler further comprises:

2   a cancel generator coupled to the matching circuit to generate a

3   cancellation request to the prefetcher when the current prefetch address matches

4   to the at least P of the stored prefetch addresses.

1   6.   The apparatus of claim 4 wherein the matching circuit comprises:

2   a plurality of comparators to compare the current prefetch address with

3   each of the stored prefetch addresses.

1   7.   The apparatus of claim 4 wherein the matching circuit comprises:

2   a plurality of comparators to compare the current prefetch address with

3   contents of the plurality of registers, the comparators generating comparison

4   results.

1   8.   The apparatus of claim 7 wherein the cancel generator comprises:

2   a comparator combiner coupled to the comparators to combine the

3   comparison results, the combined comparison results corresponding to the

4   cancellation request.

1   9.   The apparatus of claim 2 wherein the canceler comprises:

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2   a matching circuit having an argument register to store the current

3 prefetch address for matching with entries of the CAM.

1   10. The apparatus of claim 9 wherein the canceler further comprises:

2   a cancellation generator to generate a match indicator when the current

3 prefetch address matches at least P of the entries, the match indicator

4 corresponding to the cancellation request.

1   11. A method comprising:

2   storing a plurality of prefetch addresses in a storage circuit, the plurality

3 of prefetch addresses corresponding to most recent access requests from a

4 processor, the prefetcher generating an access request to a memory when

5 requested by the processor; and

6   canceling the access request when the access request corresponds to at

7 least P of the stored prefetch addresses, P being a non-zero integer.

1   12. The method of claim 11 wherein storing comprises:

2   storing the plurality of prefetch addresses in one of a queue with a

3 predetermined size and a content addressable memory (CAM).

1   13. The method of claim 12 wherein storing the plurality of prefetch

2 addresses in the queue comprises:

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3   storing the plurality of prefetch addresses in a plurality of registers
4   cascaded to shift the prefetch addresses each time the processor generates a
5   prefetch request.

1   14.   The method of claim 13 wherein canceling comprises:

2   matching a current prefetch address associated with the access request
3   with the stored prefetch addresses.

1   15.   The method of claim 14 wherein canceling further comprises:

2   generating a cancellation request to the prefetcher when the current
3   prefetch address matches to the at least P of the stored prefetch addresses.

1   16.   The method of claim 14 wherein matching comprises:

2   comparing the current prefetch address with each of the stored prefetch
3   addresses.

1   17.   The method of claim 14 wherein matching comprises:

2   comparing the current prefetch address with contents of the plurality of
3   registers, the comparators generating comparison results.

1   18.   The method of claim 17 wherein generating the cancellation
2   request comprises:

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3   combining the comparison results, the combined comparison results

4   corresponding to the cancellation request.

19.   The method of claim 12 wherein canceling comprises:

2   storing the current prefetch address in an argument register for matching

3   with entries of the CAM.

1   20.   The method of claim 9 wherein canceling further comprises:

2   generating a match indicator when the current prefetch address matches

3   at least P of the entries, the match indicator corresponding to the cancellation

4   request.

1   21.   A system comprising:

2   a processor to generate prefetch requests;

3   a memory to store data; and

4   a chipset coupled to the processor and the memory, the chipset

5   comprising:

6   a prefetcher to generate an access request to the memory when

7   requested by the processor;

8   a prefetch monitor circuit coupled to the prefetcher, the prefetch

9   monitor circuit comprising:

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10   a storage circuit coupled to the prefetcher to store a plurality of prefetch

11   addresses, the plurality of prefetch addresses corresponding to most recent

12   access requests from the processor; and

13   a canceler coupled to the storage circuit and the prefetcher to

14   cancel the access request when the access request corresponds to

15   at least P of the stored prefetch addresses, P being a non-zero

16   integer.

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1   22.   The system of claim 21 wherein the storage circuit comprises:

2   a storage element to store the plurality of prefetch addresses from the

3   most recent access requests by the processor, the storage element being one of

4   a queue with a predetermined size and a content addressable memory (CAM).

1   23.   The system of claim 22 wherein the queue comprises:

2   a plurality of registers cascaded to shift the prefetch addresses each time

3   the processor generates an access request.

1   24.   The system of claim 23 wherein the canceler comprises:

2   a matching circuit to match a current prefetch address associated with

3   the access request with the stored prefetch addresses.

1   25.   The system of claim 24 wherein the canceler further comprises:

2   a cancel generator coupled to the matching circuit to generate a

3   cancellation request to the prefetcher when the current prefetch address matches

4   to the at least P of the stored prefetch addresses.

1   26.   The system of claim 24 wherein the matching circuit comprises:

2   a plurality of comparators to compare the current prefetch address with

3   each of the stored prefetch addresses.

1   27.   The system of claim 24 wherein the matching circuit comprises:

2   a plurality of comparators to compare the current prefetch address with

3   contents of the plurality of registers, the comparators generating comparison

4   results.

1   28.   The system of claim 27 wherein the cancel generator comprises:

2   a comparator combiner coupled to the comparators to combine the

3   comparison results, the combined comparison results corresponding to the

4   cancellation request.

1   29.   The system of claim 22 wherein the canceler comprises:

2   a matching circuit having an argument register to store the current

3   prefetch address for matching with entries of the CAM.

1   30.   The system of claim 29 wherein the canceler further comprises:

2   a cancellation generator to generate a match indicator when the current

3   prefetch address matches at least P of the entries, the match indicator

4   corresponding to the cancellation request.